UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,140	12/31/2003	Yoshihiro Izumi	925-280	6877

23117 7590 10/04/2005

NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
SCHECHTER, ANDREW M	
ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/748,140	IZUMI ET AL.
	Examiner	Art Unit
	Andrew Schechter	2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-11,13 and 14* is/are pending in the application.

4a) Of the above claim(s) *14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-11 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/863,266.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 16 September 2005 have been fully considered but they are not persuasive.

The submission of the Rule 131 Declaration removes *Tsujimura* as prior art, so the previous rejections in view of *Tsujimura* have been withdrawn.

As requested by the applicant, the examiner has considered the reference *Takemura,* U.S. Patent No. 5,757,444 and deems it to be relevant as discussed below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 9-11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Yoritomi et al.,* Japanese Patent Document No. 04-081820 in view of *Takemura,* U.S. Patent No. 5,757,444, and further in view of *Tagusa et al.*, U.S. Patent No. 5,946,065.

[The examiner consulted a translator regarding the *Yoritomi* reference; page references are to the original Japanese text. The PTO will provide a full translation of the reference with the next office action (if desired).]

Yoritomi discloses [see Figs. 1-4] a method of making an active matrix substrate, the method comprising forming switching elements disposed in a shape of a matrix [see Figs. 2-3, for instance], gate signal lines [9, 2] controlling the switching elements and extending in a first direction, and source signal lines [10, 5] connected to the switching elements and extending in a second direction perpendicular to the first direction on a front surface of a light permeable substrate [1, transparent glass, see p. 2]; forming a negative type photosensitive transparent conductive material [see abstract] whose exposed parts are left in a pattern, by developing the negative type photosensitive transparent conductive material so as to obtain pixel electrodes by removing unexposed parts of the negative type photosensitive transparent conductive material [see p. 3, the non-exposed parts are removed, leaving the pixel electrodes which have been exposed, hence it is negative type].

Yoritomi does not disclose the additional limitations of forming an interlayer insulating film on the switching elements, the gate signal lines, and the source signal lines, on which is formed the transparent conductive material; and performing exposure from a back surface side of the light permeable substrate in order to expose the negative type photosensitive transparent conductive material in a self-alignment fashion by using the gate and source signal lines as exposure masks.

Takemura discloses [see Fig. 5, for instance] forming an interlayer insulating film [409] on the analogous switching elements, the gate signal lines, and the source signal lines, on which is formed the pixel electrode [412] (which in *Yoritomi* is made of the transparent conductive material). *Takemura* may or may not provide an explicit

teaching for doing so (it appears to teach the benefit of having a larger aperture ratio – compare Figs. 2 and 4 - but this is not made clearly explicit in the text). However, *Tagusa* discloses [see Fig. 10] an analogous device with an analogous interlayer insulating film, and teaches that its existence makes the pixel electrodes flat without being influenced by steps formed by the underlying lines and switching elements, preventing electrical disconnections and disturbances of the liquid crystal molecules, and reducing the number of defective pixels caused by electrical leakage between the signal lines and the pixel electrodes [col. 22, lines 14-26]. It would therefore have been obvious to one of ordinary skill in the art at the time of the invention to form the interlayer insulating film, as done by *Takemura* and *Tagusa*, in the device of *Yoritomi*, motivated by the above teaching of *Tagusa*.

Takemura also discloses [see Fig.5C] performing exposure from a back surface side of the light permeable substrate in order to expose a negative type photosensitive material [411] in a self-alignment fashion by using the gate and source signal lines as exposure masks (in *Yoritomi*, the negative type photosensitive material is also the pixel electrode; here the negative type material is used as a mask to etch the pixel electrode).

Takemura discloses that this back exposure method, via self-alignment, allows the capacitance values C1 and C2 to be substantially equal (in other words, the pixels have substantially uniform parasitic capacitance between the pixel electrodes and the signal lines), which improves the display quality; also, the overlap of the pixel electrode and signal lines is symmetric and cross-talk can be removed [col. 7, lines 35-45]. It would have been obvious to one of ordinary skill in the art at the time of the invention to

use this back exposure method in making the device of *Yoritomi*, motivated by *Takemura's* teachings above and, since the gate and signal lines are already there, by there being no need for an additional mask, which reduces the number of manufacturing steps.

Claim 9 is therefore unpatentable.

Yoritomi discloses [see abstract, etc.] that the negative type photosensitive conductive material comprises a photosensitive resin and conductive particles of indium tin oxide dispersed in the photosensitive resin, so claims 10 and 11 are also unpatentable. The method is for making an active matrix substrate of a flat panel display, so claim 13 is also anticipated.

4. Claims 9-11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Kumagai, et al.,* Japanese Patent Document No. 2000-98367 in view of *Takemura et al.,* U.S. Patent No. 6,556,271.

Considering claim 9, *Kumagai* discloses [see machine translation provided in the office action of 4 March 2004 in application 09/863,266] a method of making an active matrix substrate comprising: forming switching elements disposed in a shape of a matrix [see paragraph 0022], gate signal lines ["scanning line" attached to gate electrode 2] controlling the switching elements, source signal lines [extended from source electrode 7] connected to the switching elements, forming an interlayer insulating film [11] on the switching elements, the gate signal lines, and the source signal lines; and forming pixel electrodes [13 and 14] over at least the interlayer insulating film and in electrical communication with respective switching elements through contact holes [12] defined in

the interlayer insulating film, wherein the pixel electrodes are comprised of a photosensitive conductive material including at least one coloring agent so that at least some of the pixel electrodes function as both pixel electrodes and color filters [14, part of the pixel electrode, is made of a "conductive color resist" with "photosensitivity", see paragraph 0040]. The pixel electrode of the claim can either be elements 13 and 14 taken together or, as shown in Fig. 10b, the ITO layer of the pixel electrode can be dispensed with, with layer 14 acting alone as the pixel electrode and color filter. *Kumagai* also discloses using a glass (light permeable) substrate.

Kumagai does not explicitly disclose the additional limitation that the source signal lines are formed orthogonal to the gate signal lines. The examiner takes official notice that it is well-known and conventional to do so, and that it would have been obvious to one of ordinary skill in the art at the time of the invention to do so with this device, motivated by the desire to make a standard rectangular array which can be driven by a standard arrangement of gate and signal line drivers at the edge of the panel, among other reasons.

Kumagai does not explicitly disclose the additional limitation that the photosensitive conductive material of the pixel electrodes has negative type photosensitivity whose exposed portions are left in a pattern, and performing exposure from a back surface side of the substrate in order to expose the negative type photosensitive transparent conductive material in a self-alignment fashion by using the gate signal lines and source signal lines as exposure masks, and developing it to obtain pixel electrodes by removing the unexposed parts.

Takemura discloses [see Fig. 5] using negative type photosensitive material [411] for an analogous layer and using the gate and source lines as masks during exposure of the material from the back side of the substrate, and then developing by removing the unexposed parts. *Takemura* discloses that this back exposure method, via self-alignment, allows the capacitance values C1 and C2 to be substantially equal (in other words, the pixels have substantially uniform parasitic capacitance between the pixel electrodes and the signal lines), which improves the display quality; also, the overlap of the pixel electrode and signal lines is symmetric and cross-talk can be removed [col. 7, lines 35-45]. It would have been obvious to one of ordinary skill in the art at the time of the invention to use this back exposure method in making the device of *Kumagai*, motivated by *Takemura's* teachings above and, since the gate and signal lines are already there, by there being no need for an additional mask, which reduces the number of manufacturing steps.

Claim 9 is therefore unpatentable.

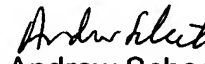
Kumagai's photosensitive conductive material comprises photosensitive resin and conductive particles of indium tin oxide (ITO) dispersed therein [see paragraph 0056], so claims 10 and 11 are also unpatentable. *Kumagai* discloses making a flat panel display device with this active matrix substrate, so claim 13 is also unpatentable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Andrew Schechter
Primary Examiner
Technology Center 2800
30 September 2005